

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory//PEG/Display	3~4
CPU-Control/MI SC/CFG/Audio	5
Power/GND	6~7
DDR4 SLOT-DIMM1~4	8~9
DDR4-POWER/GND	10~11
PCH-USB/PCIE/DMI/SATA	12
PCH-Audio/Display/Clock	13
PCH-GPIO/USBOC#/SATASTRAP	14
PCH-LPC/SPI/SMBUS/MISC	15
PCH-Power/GND/Strap	16~18
PCIE X16/X1/X4	19~21
PCIE to PCI-ASM1083	22~23
M.2/SATA Express/SATA	24~25
USB POWER/PS2/USB2.0/USB3.0	16~29
PCIE to USB3.1-ASM1142	30~31
PCIE to LAN-I219V	32
VGA/DVI/HDMI Connector	33~35
Audio-ALC1150	36~38
SIO-NCT6793D	39~40
CPU FAN/SYSTEM FAN	41~42
ATX Power/F_Panel	43
ACPI-UIP Power	44
OV-NCT3933	45
+ 12VIN/VRM_EN&PGD	46
IMVP8-PWM-ISL95858 VCORE+VGT	47~49
CPU PWR_VCCIO-NB685	50
CPU PWR_ST/PLL-GS7166/GS7116	51
CPU PWR_SA-RT8125C	52
DDR4 Power-RT8125C	53
DDR4 Power-VPP25	54
PCH Core Power-RT8125C	55
BIOS &Clear CMOS	56
Manual parts/EMI CAP	57~58
GPIO MAP	59
Power Map	60
Power Sequence	61
Revision History	62

MS-7A11

ATX

Ver: 1.1

Intel -Skylake plamform Z170

CPU:

Skylake-S

System Chipset:

Z170

Onboard Chip:

HD Audio Codec:ALC1150

LAN:Intel I219V

SIO:Nuvoton 6793D

Flash ROM: SPI 64MB /128MB(For H170/B150)

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UIP

PWM:

IMVP8 -ISL95856

Expansion Slots:

*PCI Express (X16) Slot *1*

*PCI Express (X8) Slot * 1*

*PCI Express (X4) Slot * 1*

*PCI Express (X1) Slot * 3*

*PCI Slot * 1*

*M2 * 1*

SATAe 1*

SATA3.0 x6

Other:

*REAR USB2.0 *2*

*REAR USB3.0 *4*

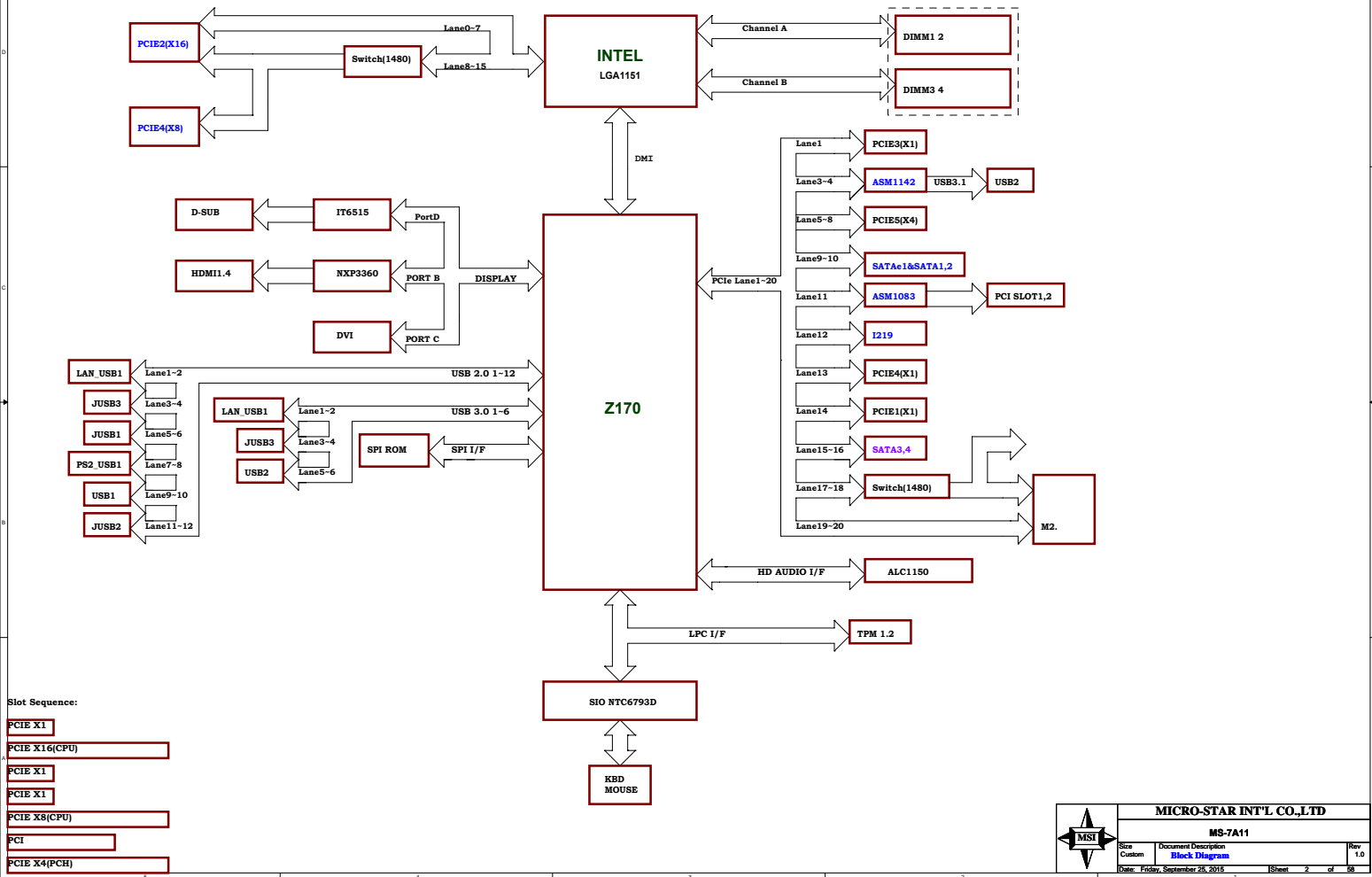
*REAR USB3.1 *2*

*FRONT USB2.0 *4*

*FRONTUSB3.0 *2*

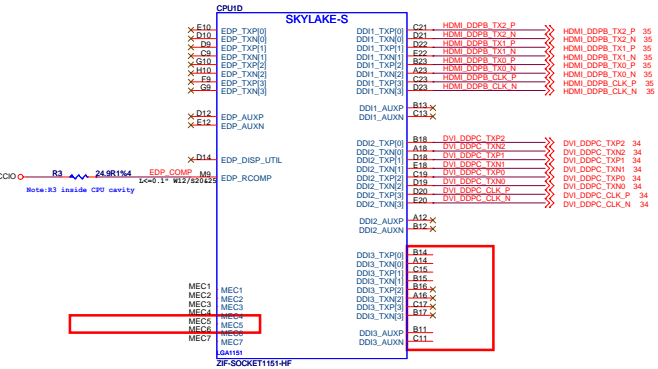
MICRO-STAR INT'L CO.,LTD			
MS-7A11			
Size	Document Description	Rev	
Custom	Cover Sheet	1.0	
Date: Friday, September 26, 2015	15Sheet	1	of 62

MS-7A11 Block Diagram



Slot Sequence:

- PCIe X1
- PCIe X16(CPU)
- PCIe X1
- PCIe X1
- PCIe X8(CPU)
- PCI
- PCIe X4(PCH)



CPU Socket MECS Hole top layer add Soldermask, bot layer not add Soldermask.
 1. MECS connect to GND.
 2. Add CPU1L.
 3. Footprint change to ZIF_SOCK1151_TEST_7978.

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MS-7A11

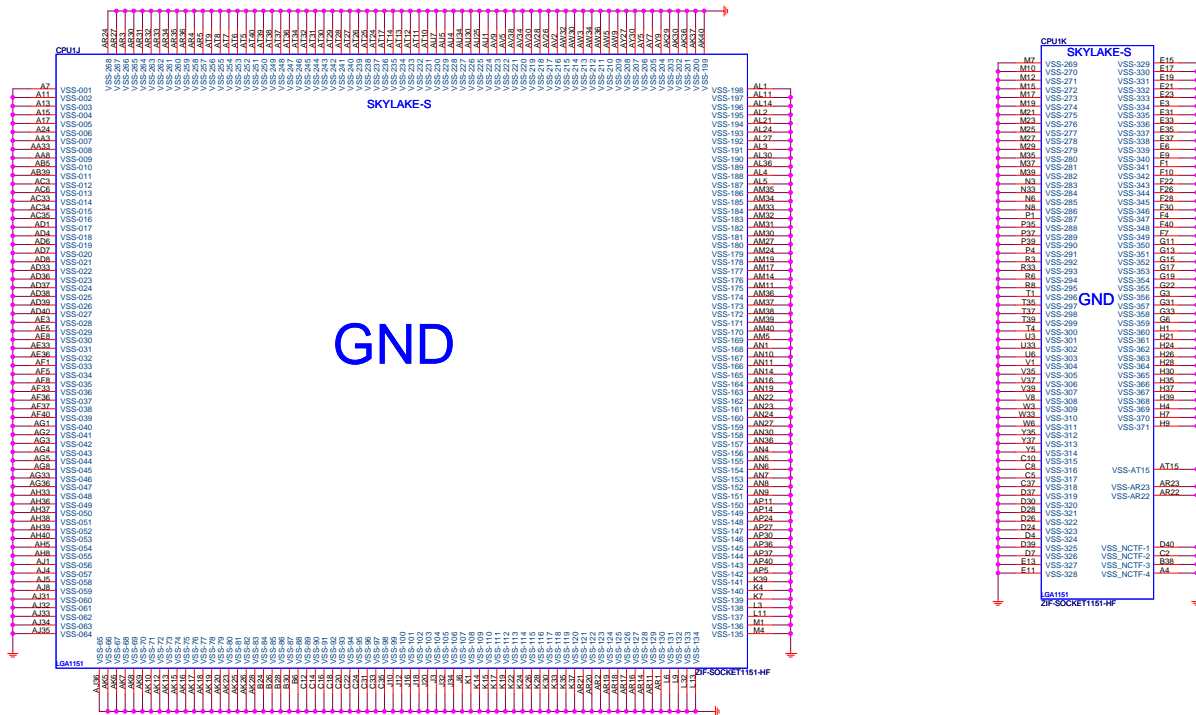
Rev: 1.0

Doc: Friday, September 26, 2015 15:00

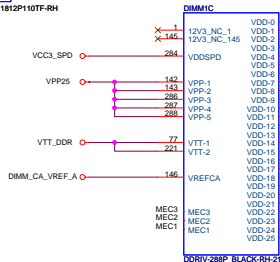
Site: Custom

Document Description: CPU-PEG/Display

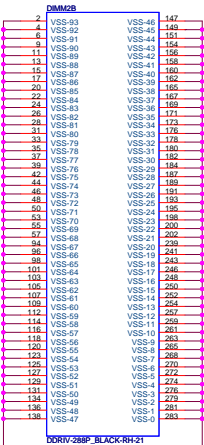
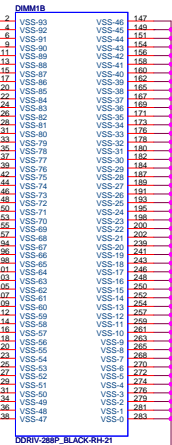
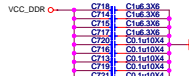
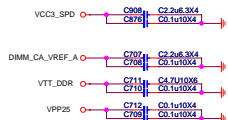
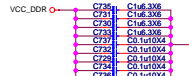
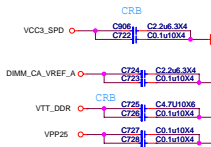
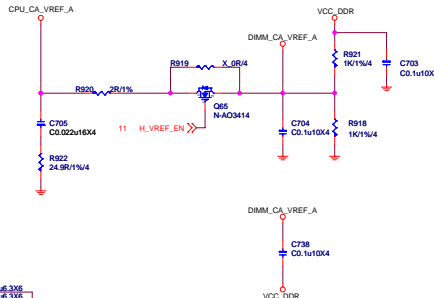
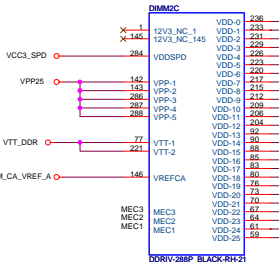
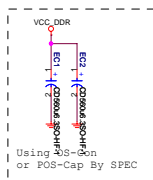
Rev: 1.0



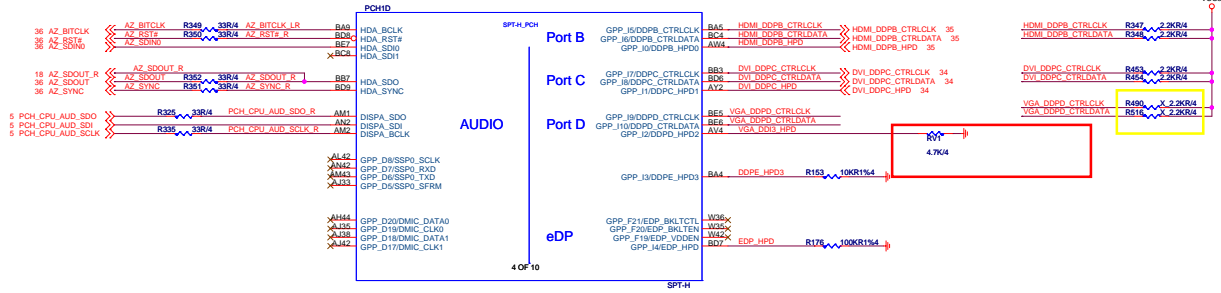
F7
VCC3_1 2 VCC3_SPD
F-SMD1812P10TF-RH



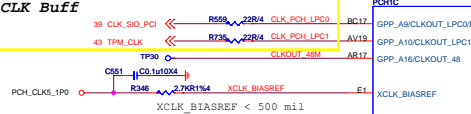
DIMM SLOT PN BY SPEC



GPP_I[3:0] with SMI/NMI



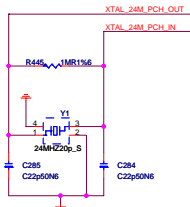
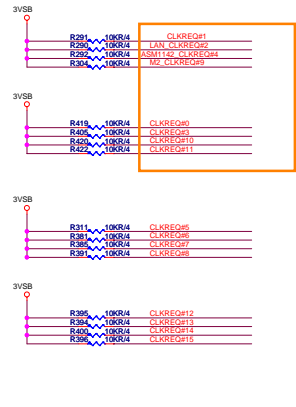
Remove CLK Buff

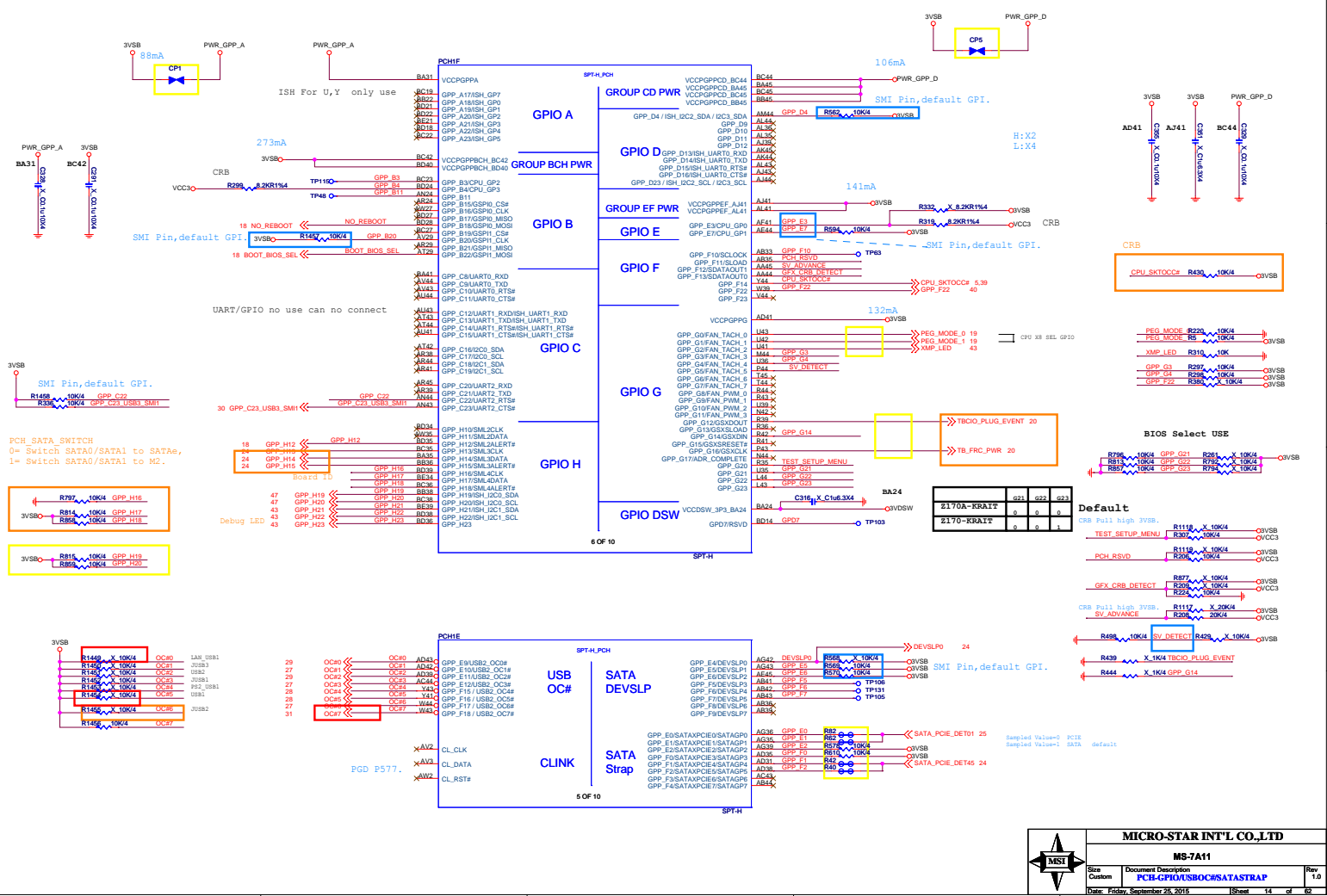


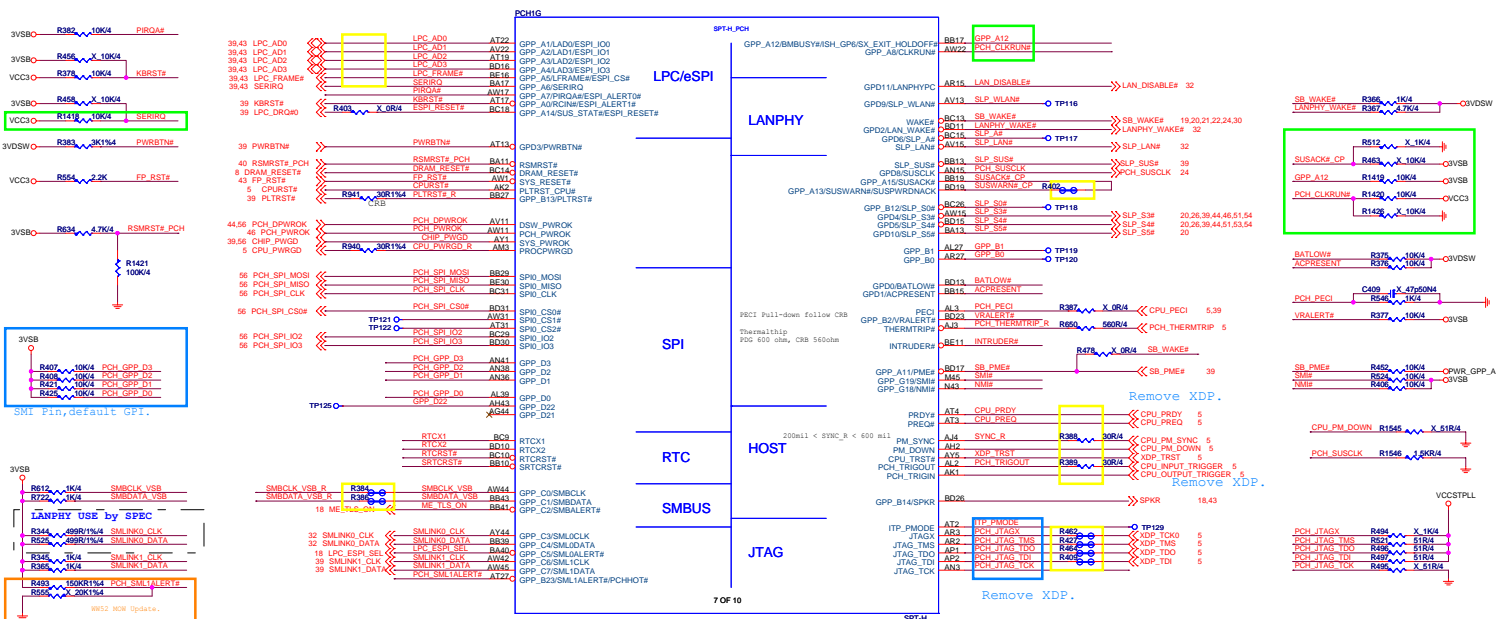
Clock

PDG #543611 Page542

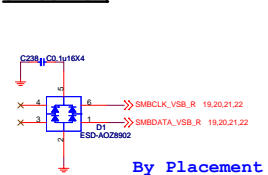
3 OF 10



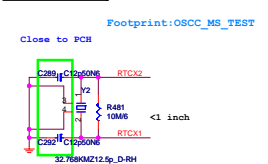




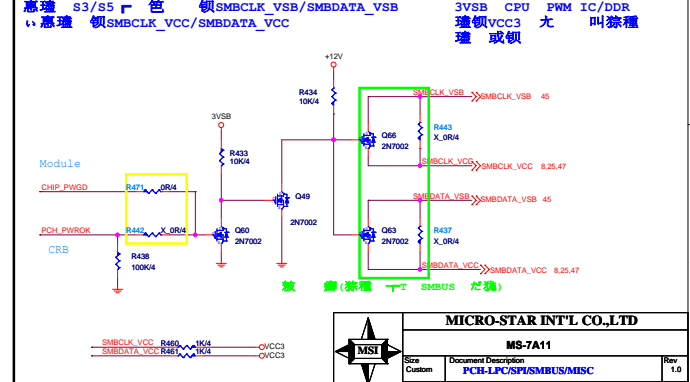
SMBUS_ESD



RTC Block

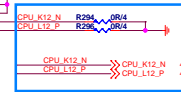
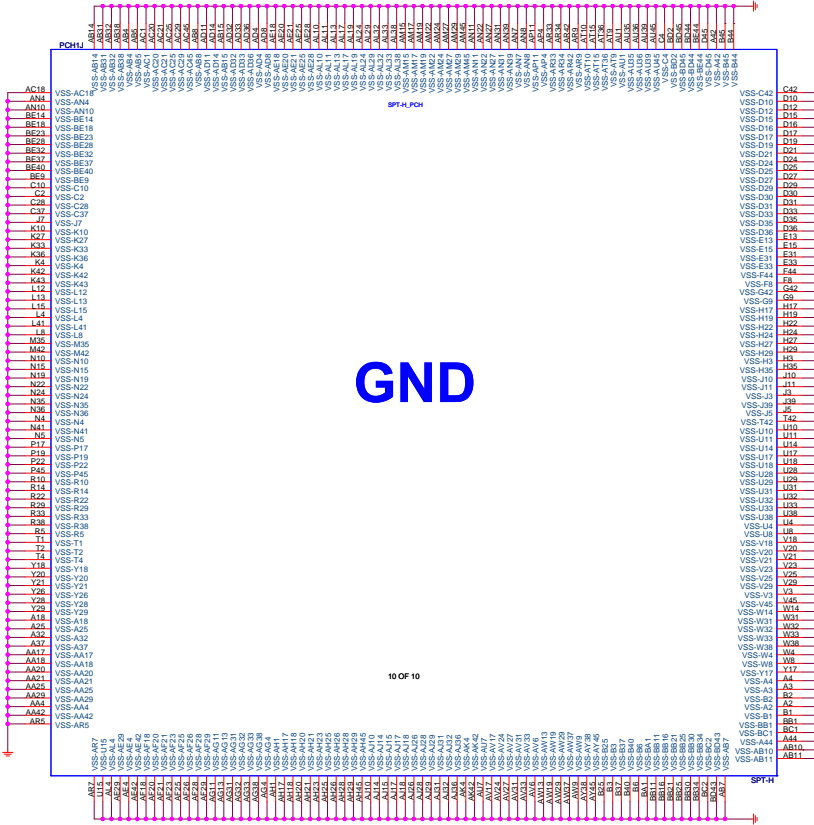


SMBUS 连接规格 (PCB 设计参考)

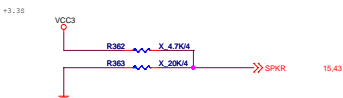


GND

10 OF 10

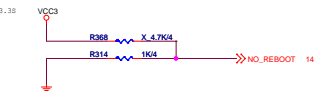


TOP Swap



Internal pull-down is disabled after PLTRST#

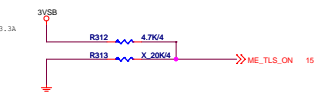
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

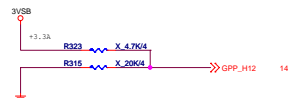
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

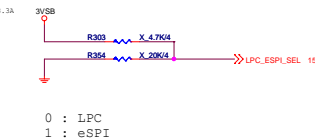
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

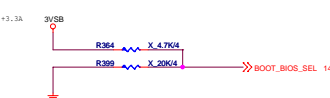
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

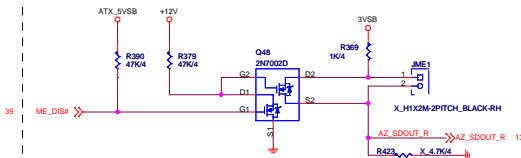
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

HDA_SDO



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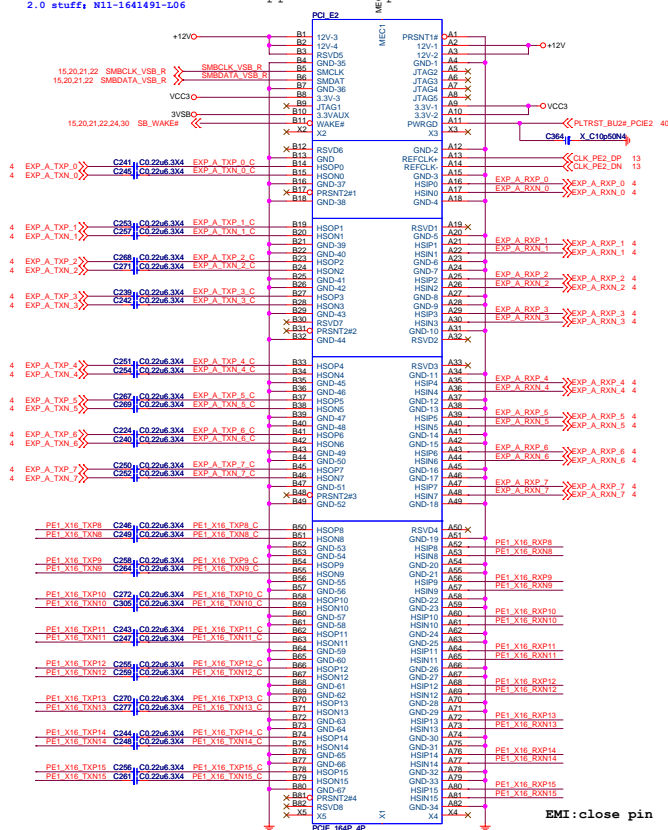
MS-7A11

Size	Document Description	Rev
Custom	PCB-Setup	1.0
Date: Friday, September 25, 2015		Sheet 18 of 62

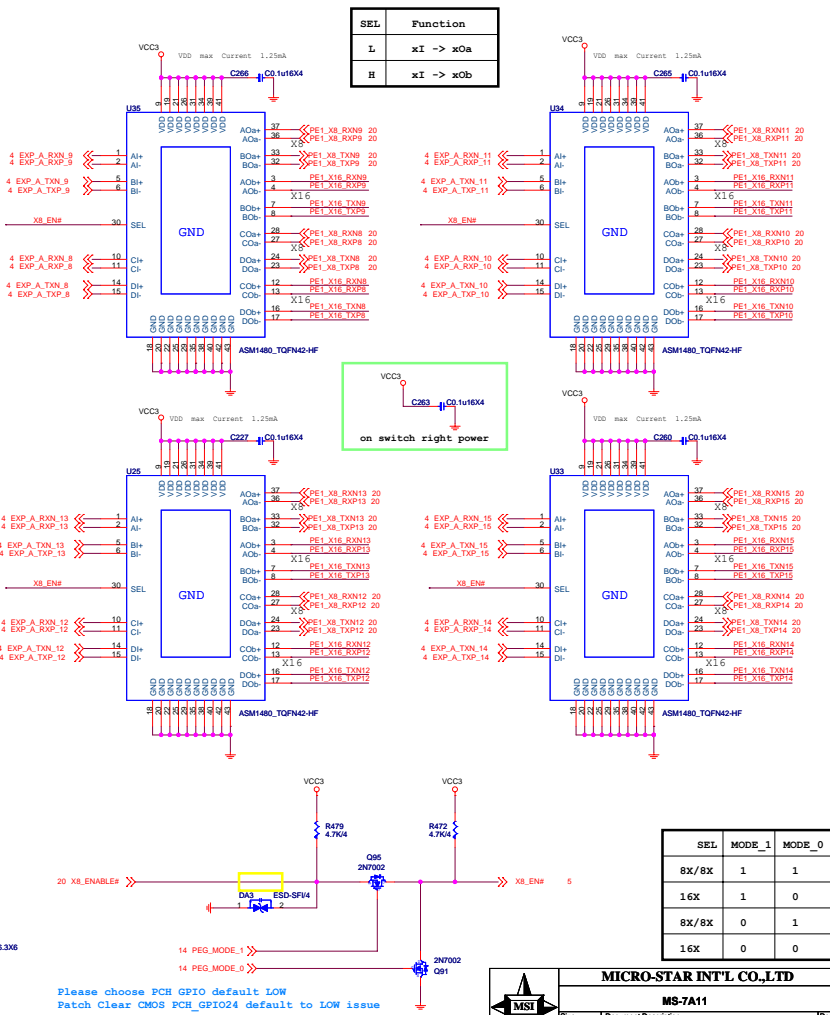
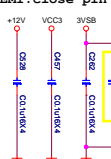
footprints: ON1-7968002
 1.0 stuff: N11-1641221-L06
 2.0 stuff: N11-1641491-L06

PCI Express X16 Slot

support max speed GEN3 Black



EMI: close pin



SEL	Function
L	xI -> x0a
H	xI -> x0b

SEL	MODE_1	MODE_0
8X/8X	1	1
16X	1	0
8X/8X	0	1
16X	0	0



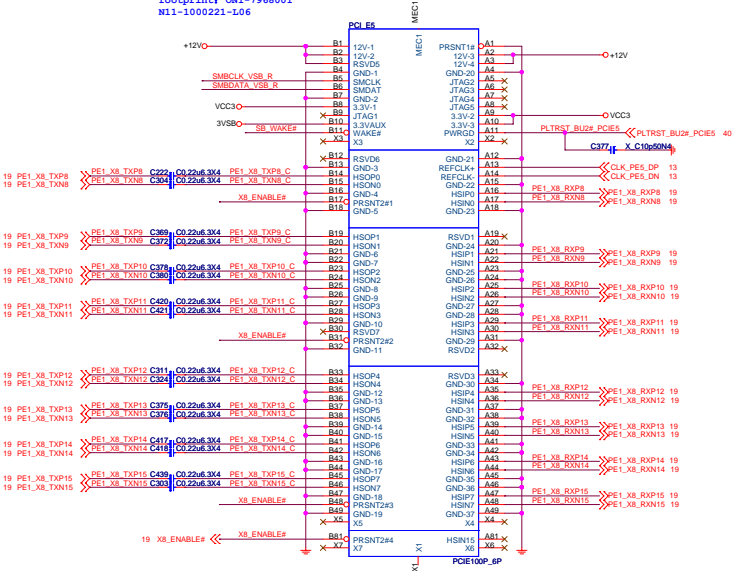
Please choose PCH GPIO default LOW
 Patch Clear CMOS PCH_GPIO24 default to LOW issue

PCI Express X8 Slot

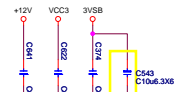
support max speed GEN3

Black

footprint: CN1-7968001
N11-1000221-1-06



EMI:close pin

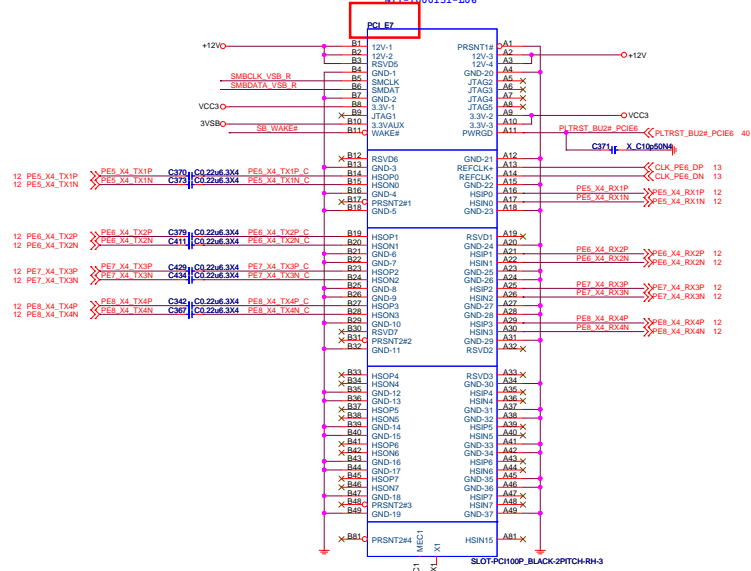


PCI Express X4 Slot

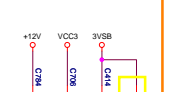
support max speed GEN3

Black

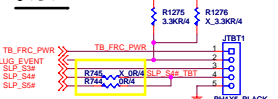
N11-1000151-1-06

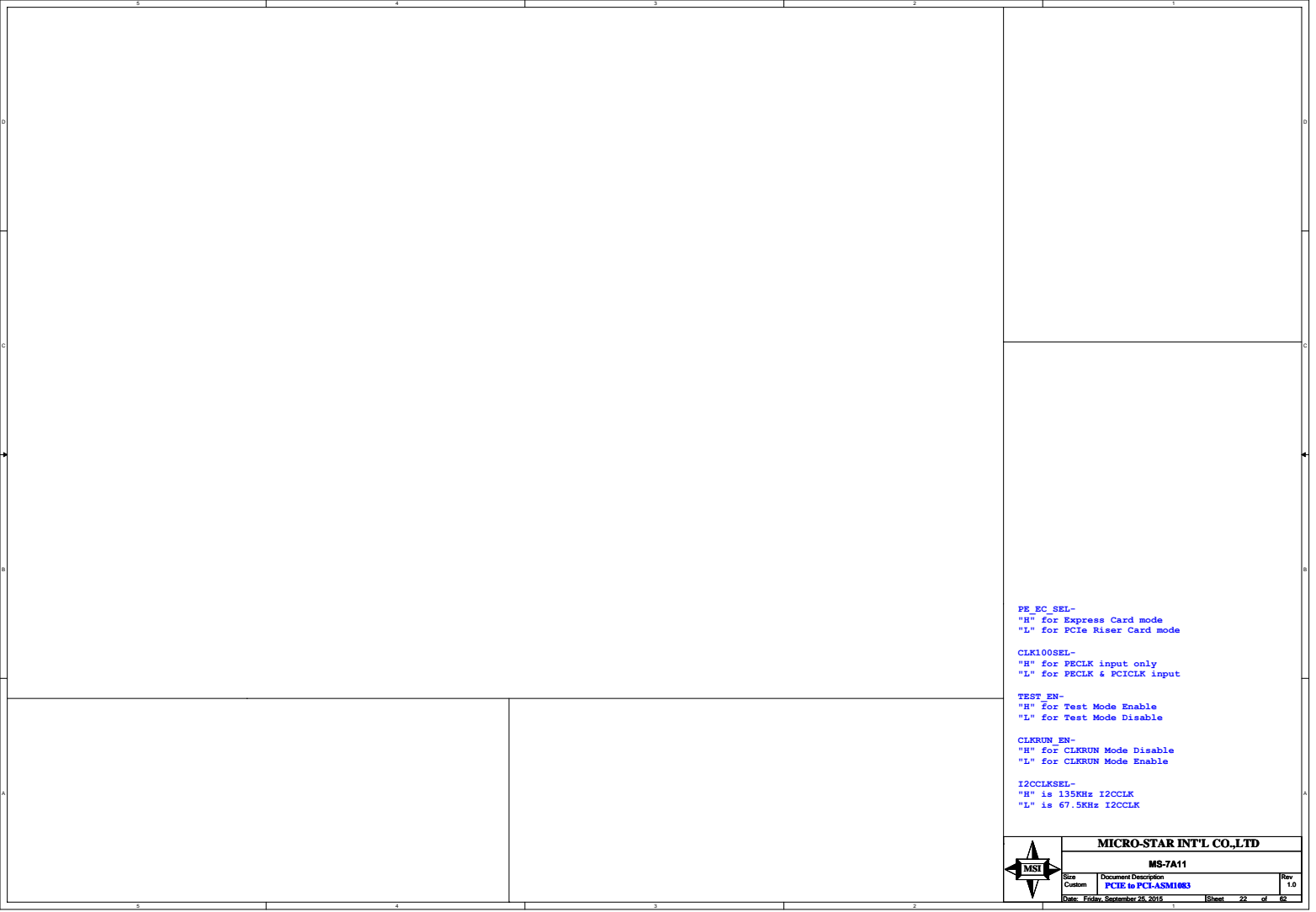


EMI:close pin



JTBT





PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK




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MS-7A11

Size	Document Description	Rev
Custom	PCIe to PCI-ASMI083	1.0

PCI slot (X3)		
+3.3Vaux	(wake)	- 1125mA
+3.3Vaux	(no wake)	- 60mA
+3.3V		- 7.6A
+5V		- 15A
+12V		- 1.5A

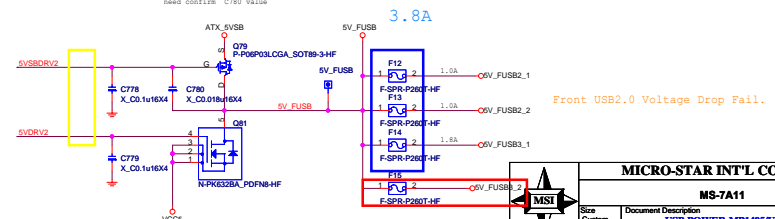
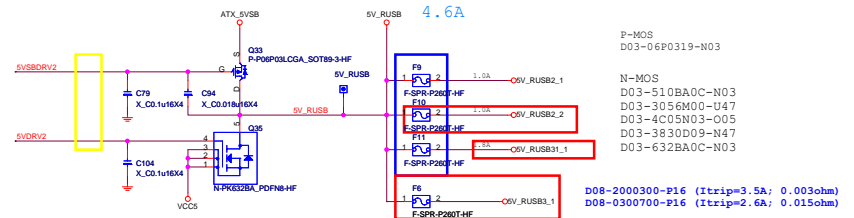
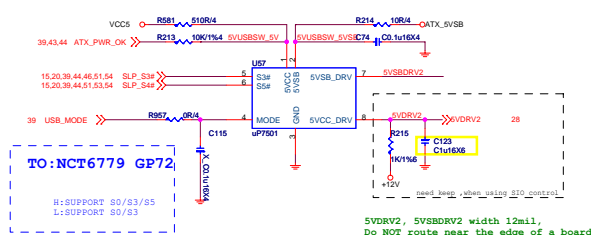


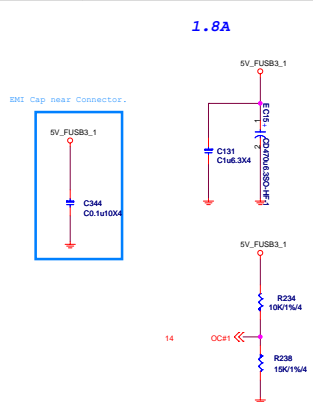
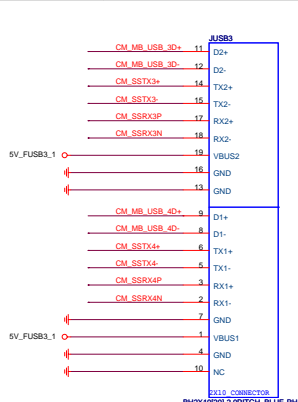
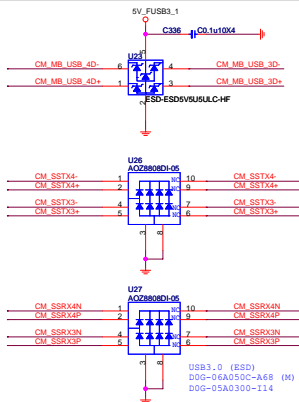
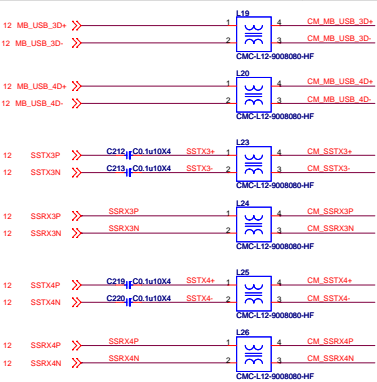
MICRO-STAR INT'L CO.,LTD		
MS-7A11		
Size Custom	Document Description PCI SLOT	Rev 1.0
Date: Friday, September 28, 2016		Sheet: 23 of 62

REAR USB PORT POWER

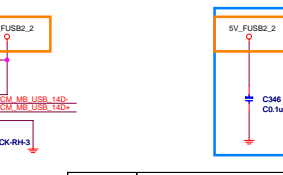
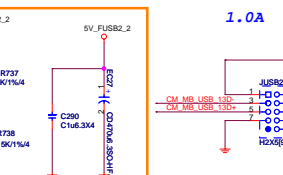
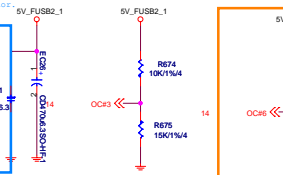
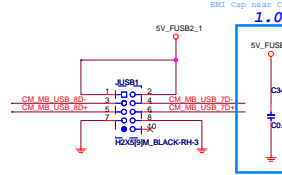
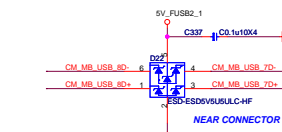
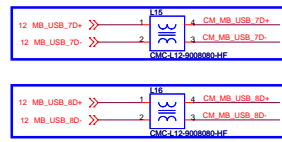
P-MOS		
D03-06P0319-N03	2A Fuse (1812)	
N-MOS		
D03-510BA0C-N03	D08-040022A-P16	
D03-3056M00-U47	D08-040021A-R02	
D03-4C05N03-O05	2A Fuse (1206)	
D03-3830D09-N47	D08-0400800-B07	
D03-632BA0C-N03	D08-0400900-L07	

(D03-P500303-N03 N/P MOS can replace Q1/Q2)

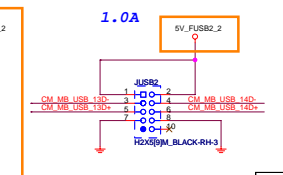
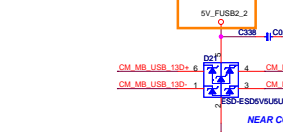
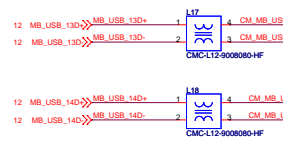




FRONT USB PORT 3,4



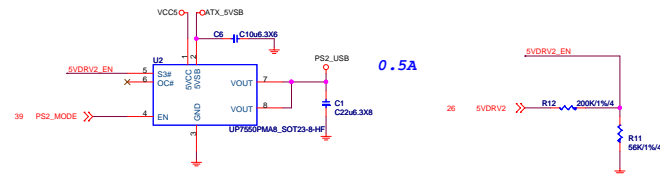
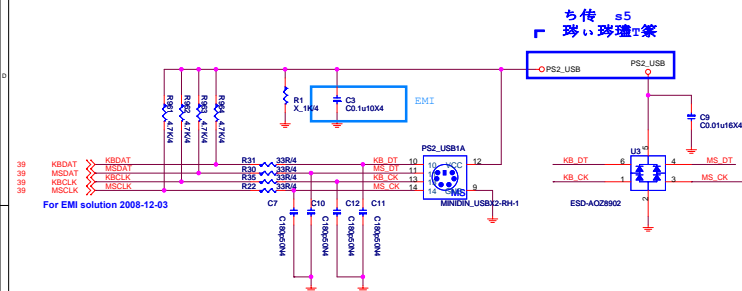
FRONT USB PORT 7,8



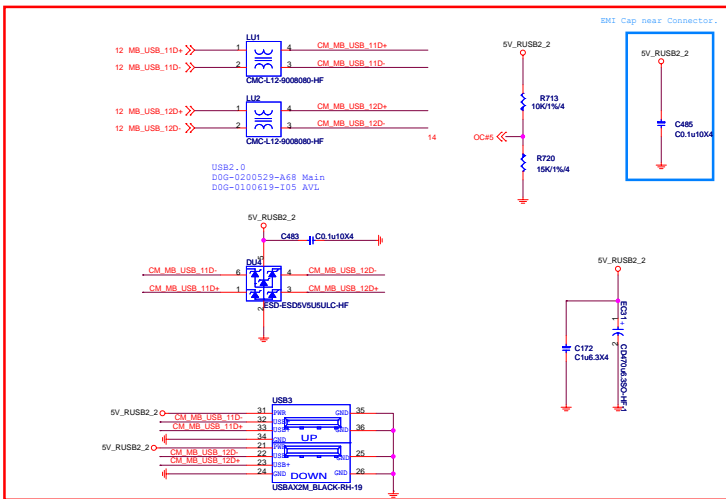
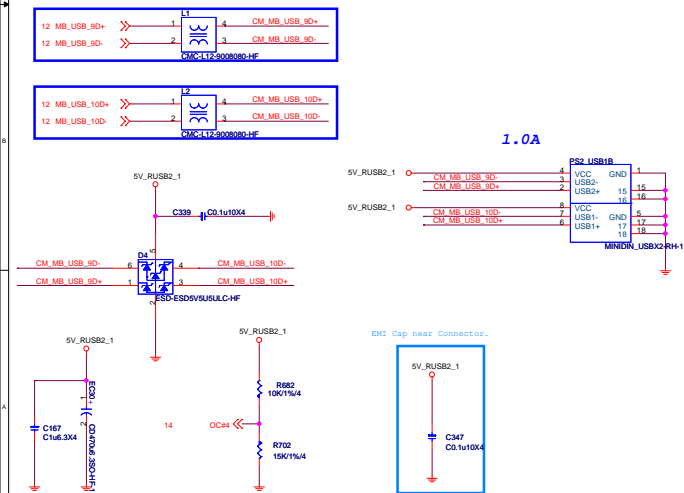
PS2 KEYBOARD & MOUSE CONNECTOR

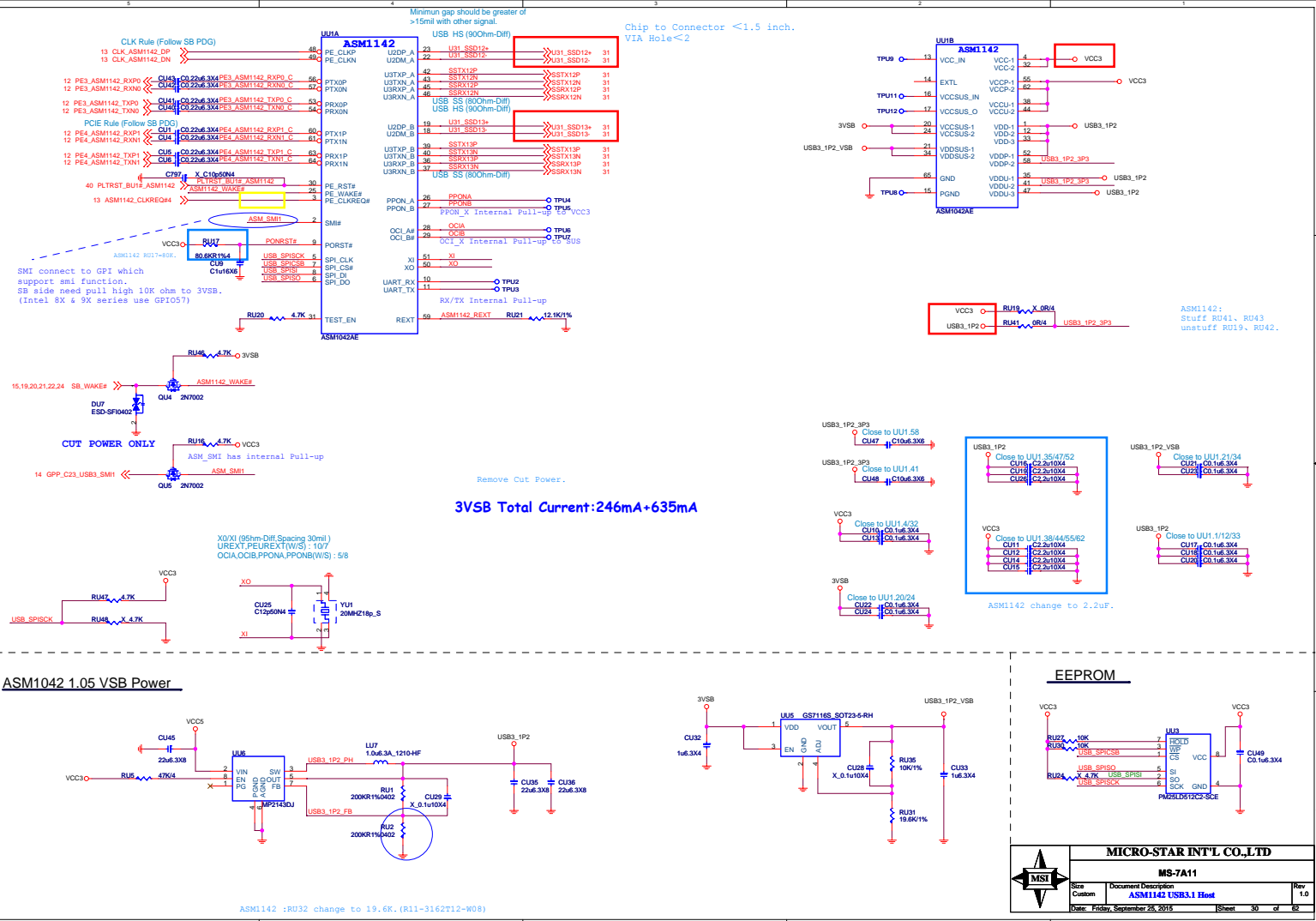
PS2 Power

USB MODE



REAR USB PORT 2,3 (W/ PS2)





Intel I219V / I218V PHY

For EMI

Reserve RL9, RL13 for Schematic Checklist

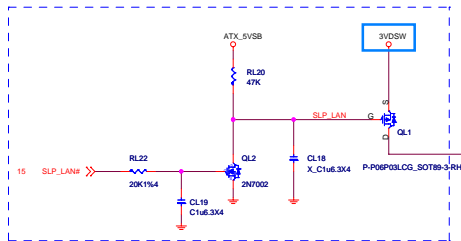
LAN_DISABLE# must be connected to PCN's LAN_P0V_P0B_CTL

PCN's PCTECLKRQ<n> port must be mapped to PCN's PET/RCn-I>port.
If CLK_RQ0_N is not used, pin#8 is pulled up 100K to 3.3V_LAN

PCN Side Pull high to 3VSB.

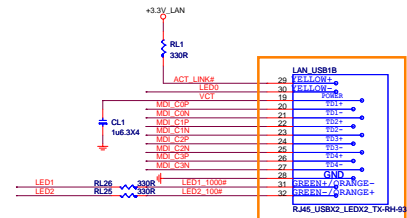
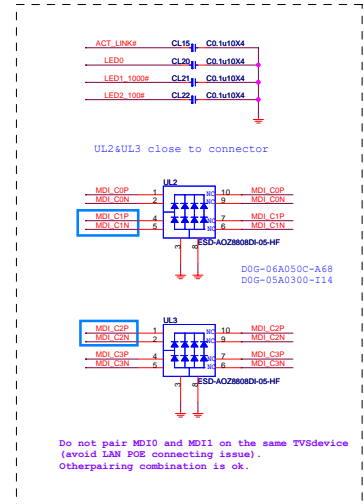
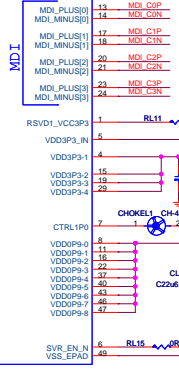
The 10kOhm pull-up resistor (RL18) of CLK_RQ0_N is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well of PCN's input PCTECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support I218/I219.



Note: These caps closed to PHY

+3.3V LAN
I218: 132mA
I219: 542mW




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MS-7A11

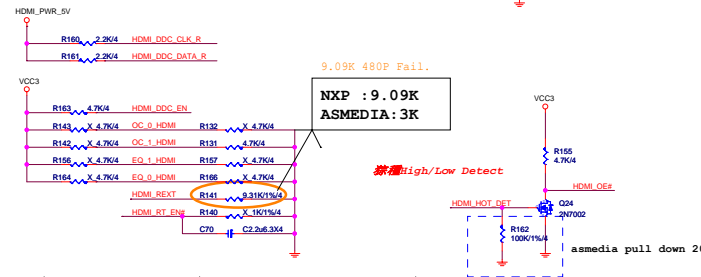
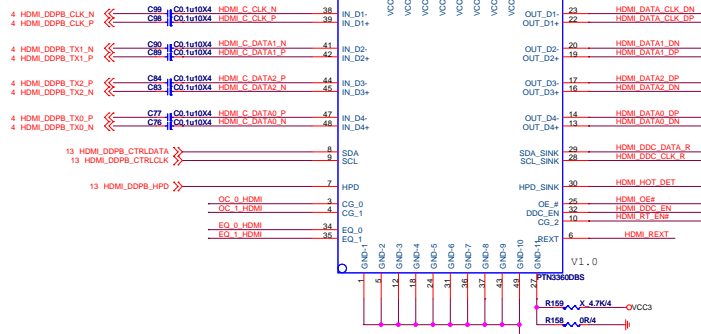
Rev	Doc	Doc	Doc
1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0





MICRO-STAR INT'L CO.,LTD		
MS-7A11		
Size	Document Description	Rev
Custom	VGA Connector	1.0
Date: Friday, September 28, 2016		Sheet 33 of 62

HDMI level shifter



	"0"	"1"
DDC_EN	DDC level shifter enable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	OE
1, 1, 0	OE	On
1, 1, 1	OE	OE
0, X, X	OE	OE

PCI, PC0	generation.	note
00	8 db	internal pull-up at ~500K ohm.
01	4 db	internal pull-down at ~500K ohm.
10	12 db	internal pull-down at ~200K ohm; 5V tolerant, internal pull-down at ~500K ohm.
11	8 db	analog current

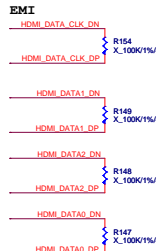
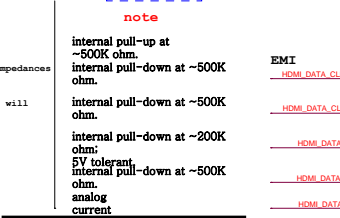
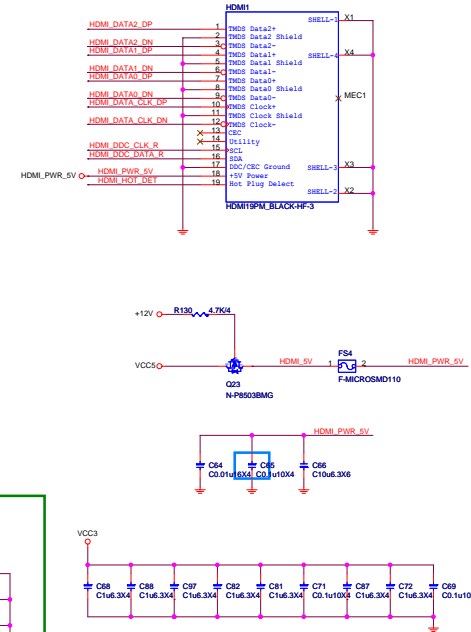


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_ON	TMD5B_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMD5B_DATA2#	DDPB_DP
	DDSP_B_TX1_ON	TMD5B_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMD5B_DATA1#	DDPB_1P
	DDSP_B_TX2_ON	TMD5B_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMD5B_DATA0#	DDPB_2P
	DDSP_B_TX3_ON	TMD5B_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMD5B_CLK#	DDPB_3P
	DDPB_HP0	DDSP_B_HP0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_B_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI_B_CTRL_DATA	





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MS-7A11

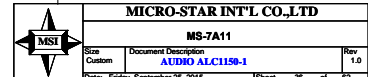
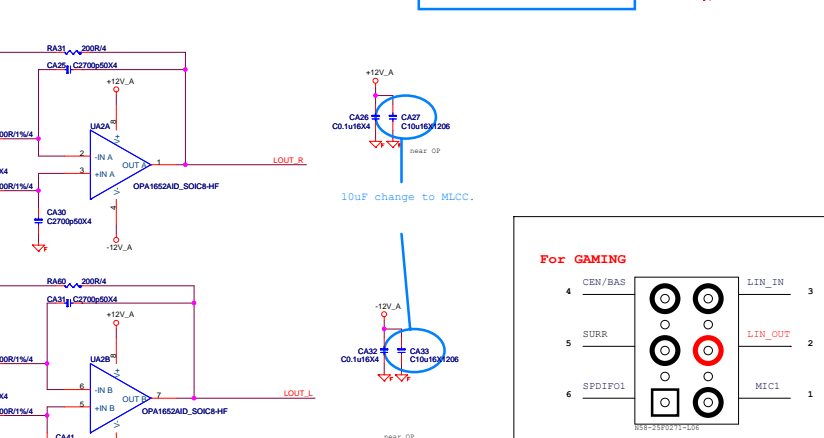
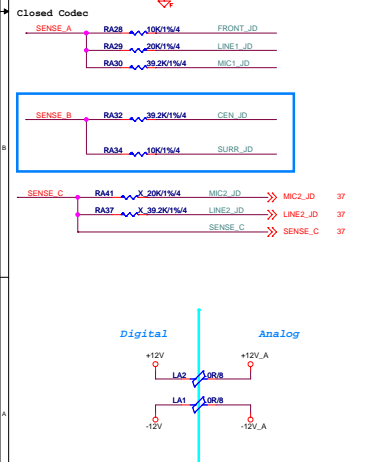
Size
Custom

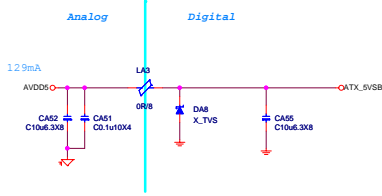
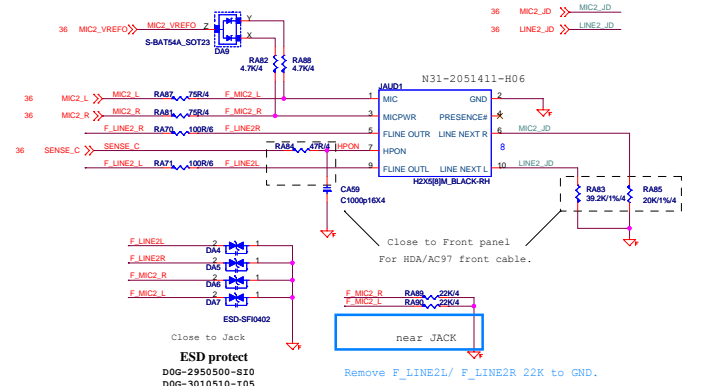
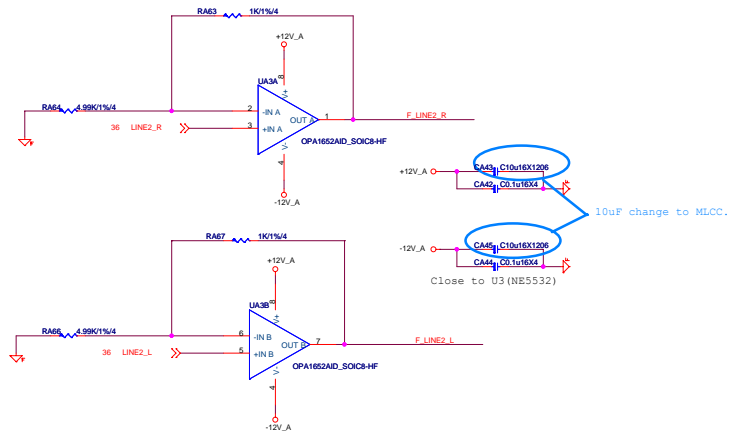
Document Description
HDMI Connector

Rev
1.0

Sheet 36 of 62

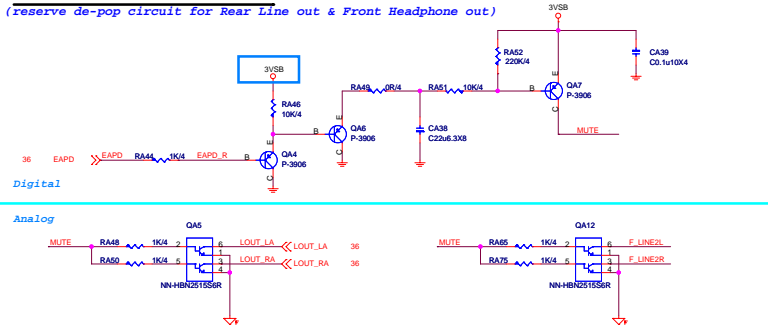
GAMING MODE



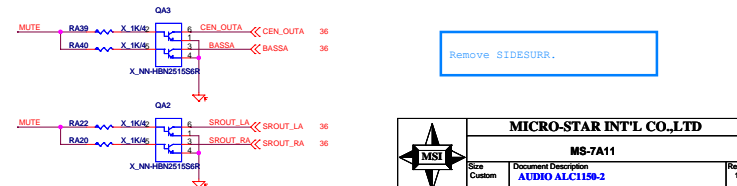


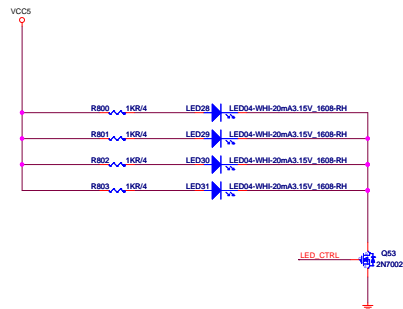
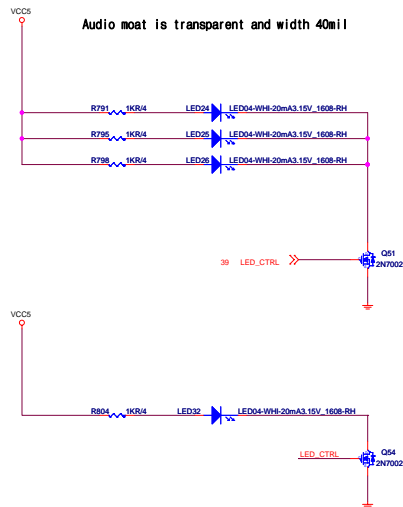
Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)

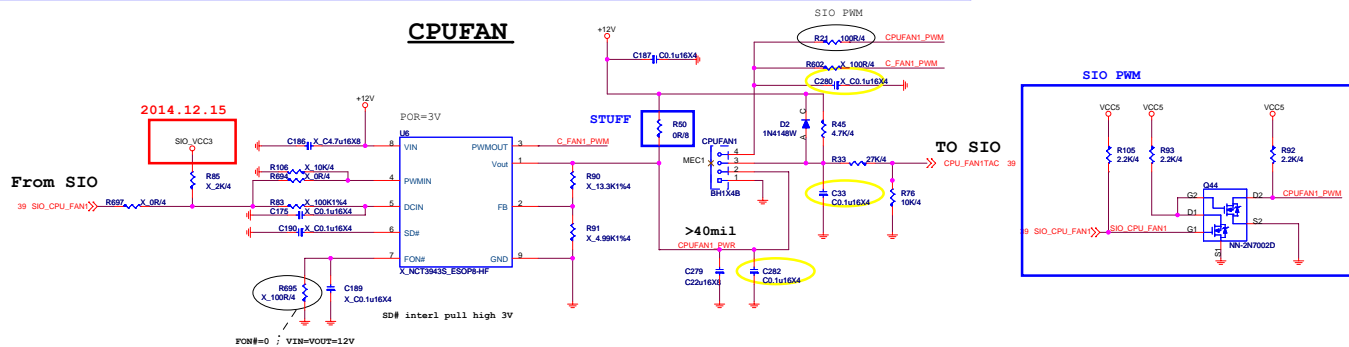


(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)

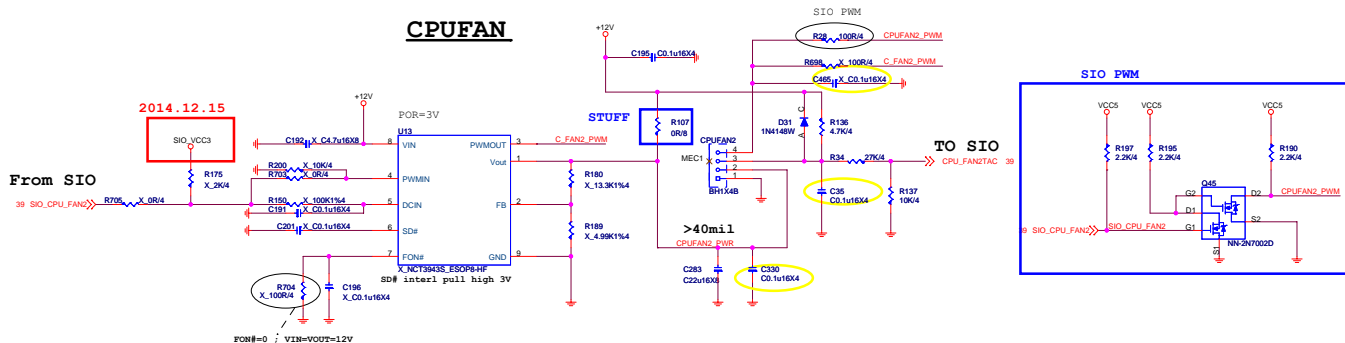




Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)

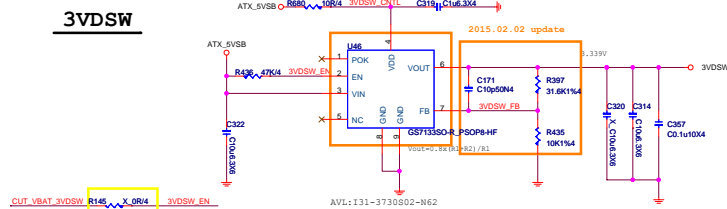


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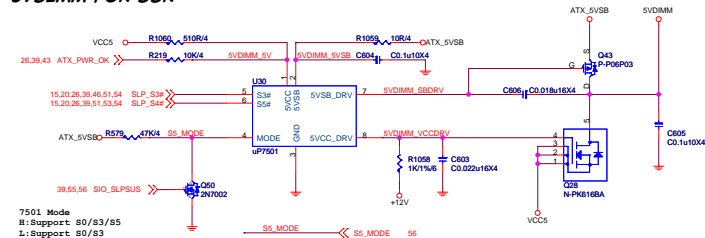
MS-7A11

Site	Customer	Document Description	Rev
		CPU FAN	1.0
Date	File	September 28, 2015	15 Item 41 of 62

3VDSW

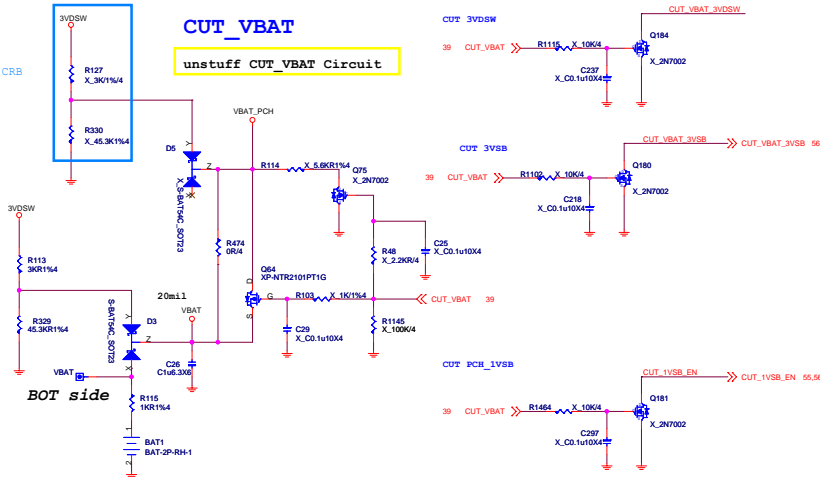


5VDIMM FOR DDR



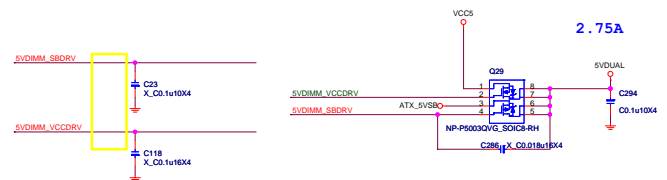
CUT VBAT

unstuff CUT VBAT Circuit



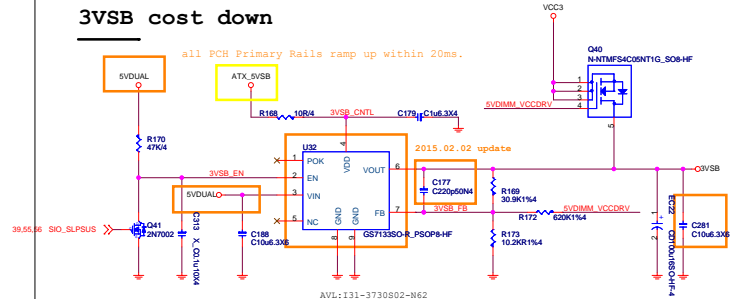
5VDUAL

SVDUAL is power source of PCH_1VSB.

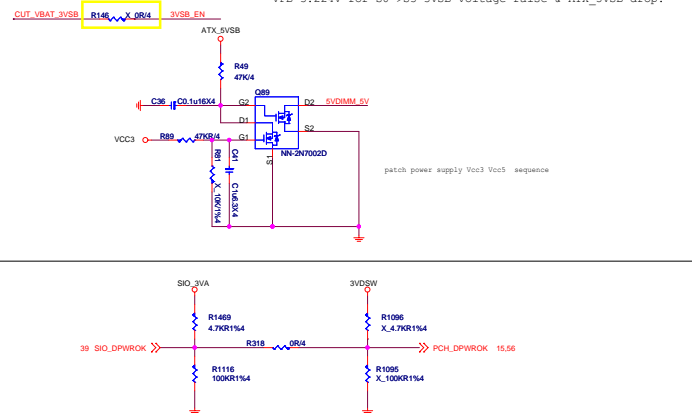


3VSB cost down

all PCH Primary Rails ramp up within 20ms.



VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.



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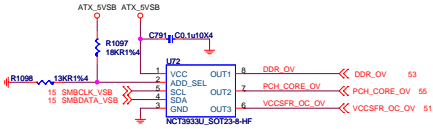
MS-7A11

Size Custom	Document Description ACPI UPI	Rev 1.0
Date: Friday, September 25, 2015		Sheet 44 of 62

Remove Cut Power.

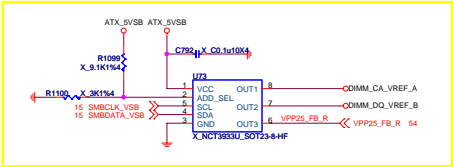
UPI VOLTAGE CONSOLE

0x28:RH=18K,RL=13K



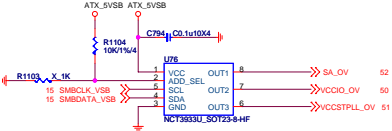
UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



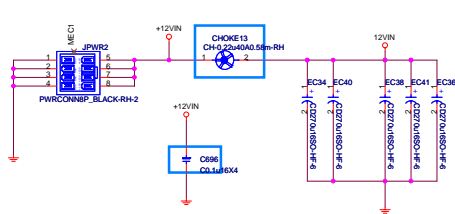
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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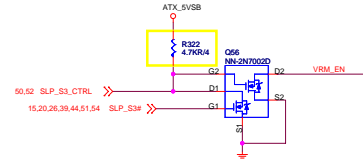
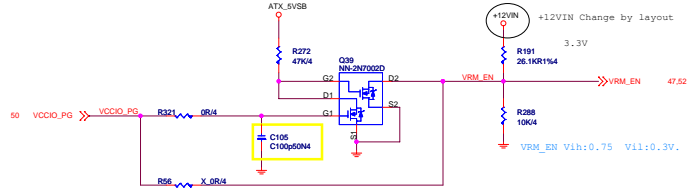
MS-7A11

Site:	Customer:	Document Description:	Rev:
		OV-NCT13933/GPIO-NCT5685	1.0
Date:	Friday, September 26, 2015	16:00	45 of 62



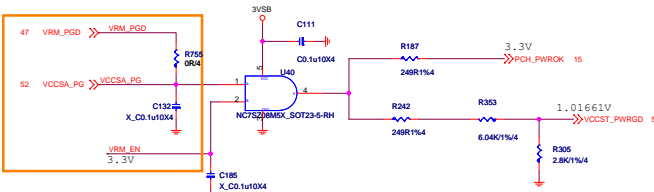
Iripple=30.95A
Vcore=18.101A
VGT=8.457A
VCCSA=4.392A

VRM_EN Control from VCCIO_PG

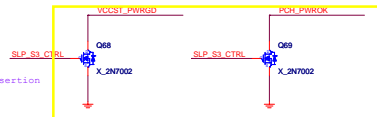


PCH_PWROR Control from VCCIO_PG&VCCSA VCCST_PWRGD Control from VRM_PGD

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC, pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROR, but must never lag it.



VCCIO使用NB681/685時, PIN 3V3要接外部VCC3,
VCCIO_PG上升時會將一根到0.6V,
所以PCH_PWROR前端的VCCIO_PG改接VRM_EN.



For VCCST_PWRGD deassertion
makilum

The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).data & clk mismatch

Route the Alert signal between the Clock and the Data signals.

Constraint: 5/10/15

SVID Addr 00h : VCORE
SVID Addr 01h : VGT
SMBus Addr: XXh

VCORE Iccmax=100A

VGT Iccmax =48A

TDP: 95W

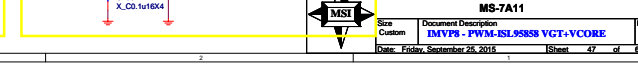
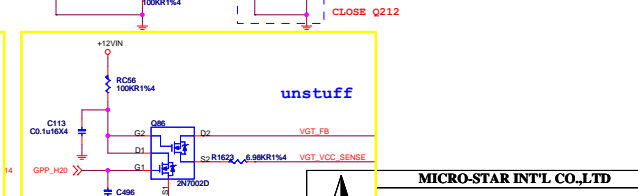
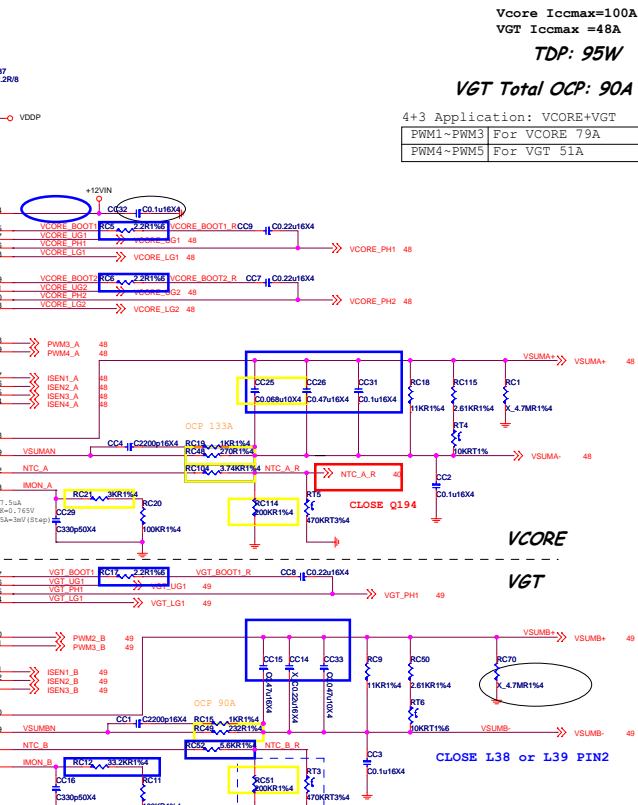
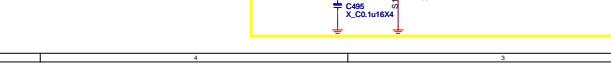
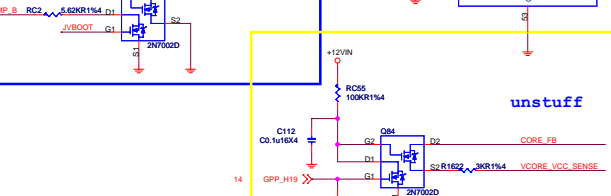
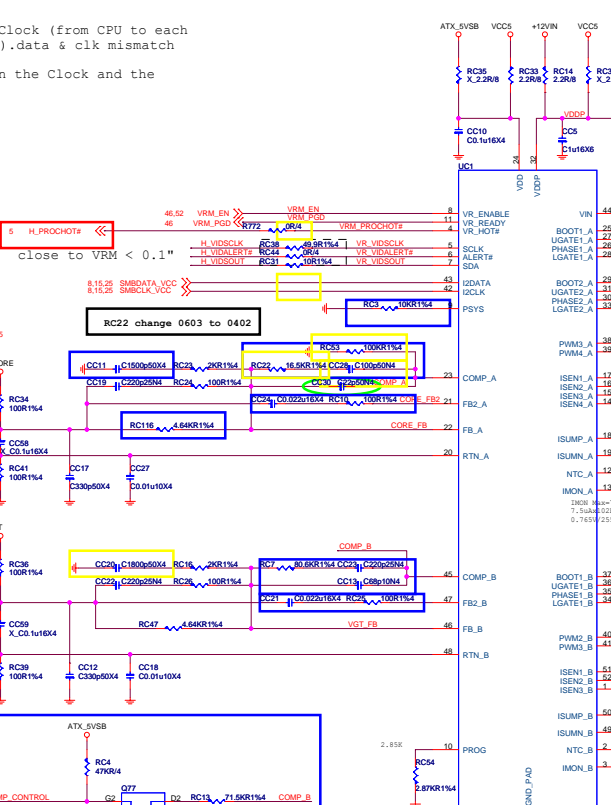
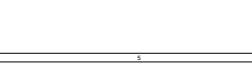
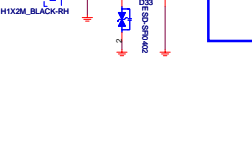
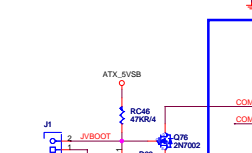
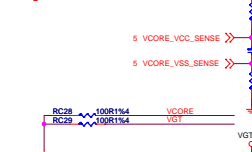
VGT Total OCP: 90A

4+3 Application: VCORE+VGT

PWM1-PWM3 For VCORE 79A

PWM4-PWM5 For VGT 51A

VCCSTPL close to VRM <0.1"



VCORE

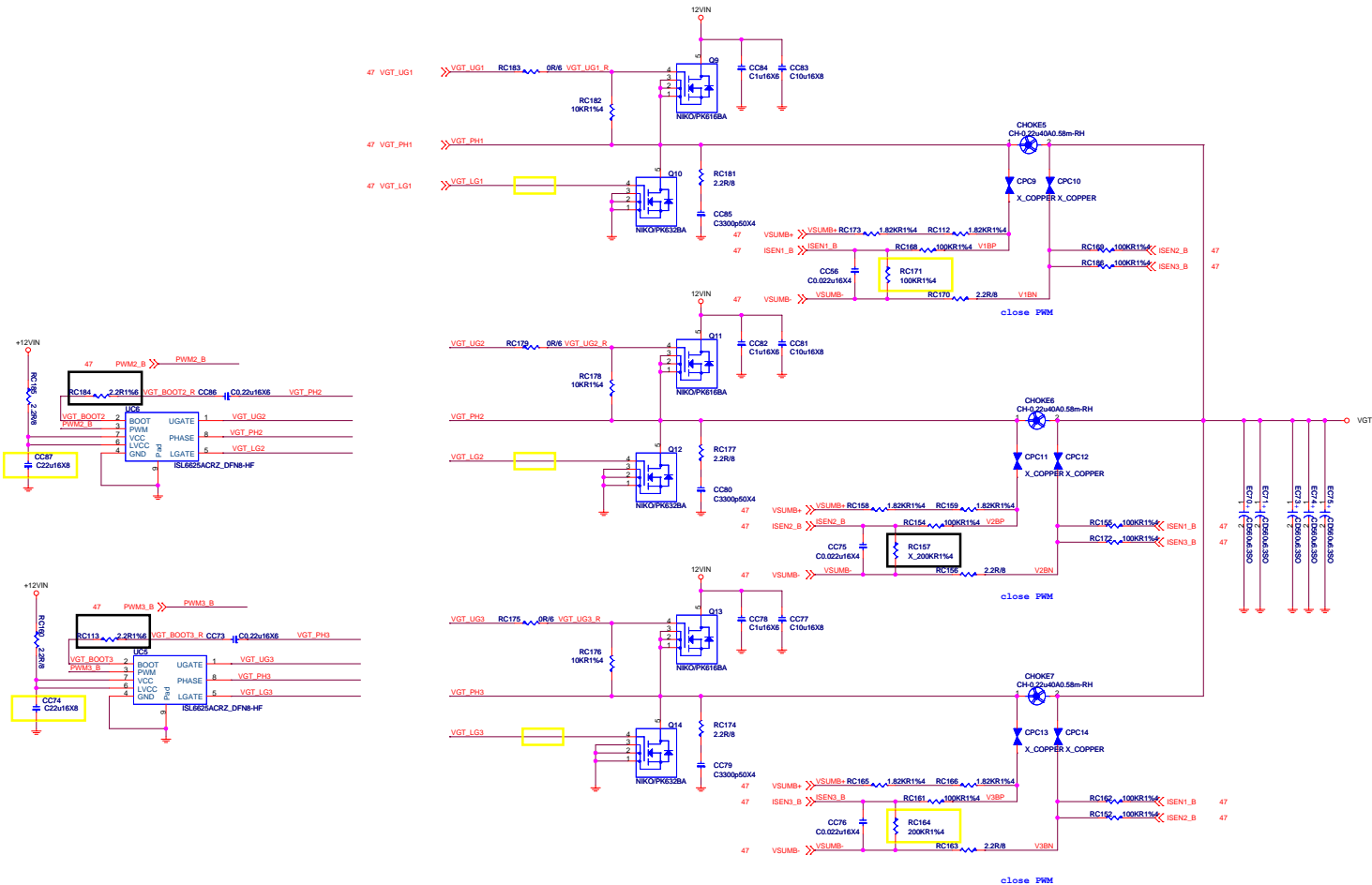
VGT

CLOSE L38 or L39 PIN2

MICRO-STAR INT'L CO.,LTD

MS-7A11

Size	Document Description	Rev
Custom	MPVS - PWMA-SL5858 VGT-VCORE	1.0
Date: Friday, September 25, 2015	Issued	47 of 62



VCCIO

0.95V; 5.5A

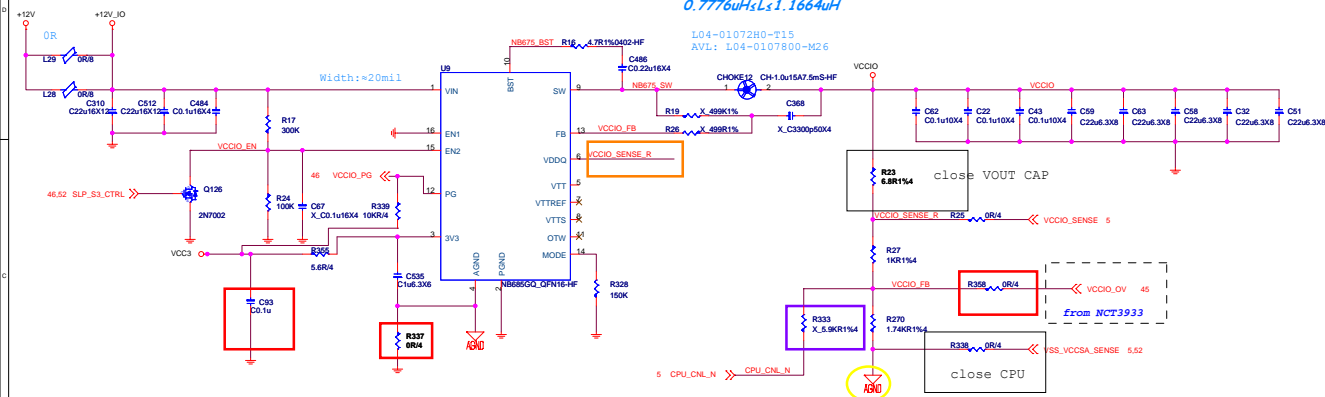
(H110 VCCIO=VCCSA)

IMAX 10A

ILIMIT=10A~12A

IOC=ILIMIT*40%*IMAX/2=12A~14A.

0.7776uHsLs1.1664uH



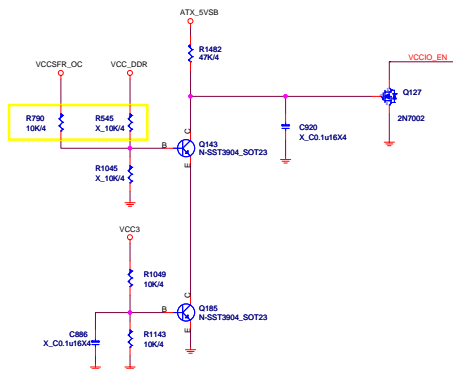
2014.08.21 update

RSVD for CRB

CPU_CNL_N come from CPU PROC_SELECT#

SLP_S3# assertion to VCCIO VR disabled $\leq 1\mu s$.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms

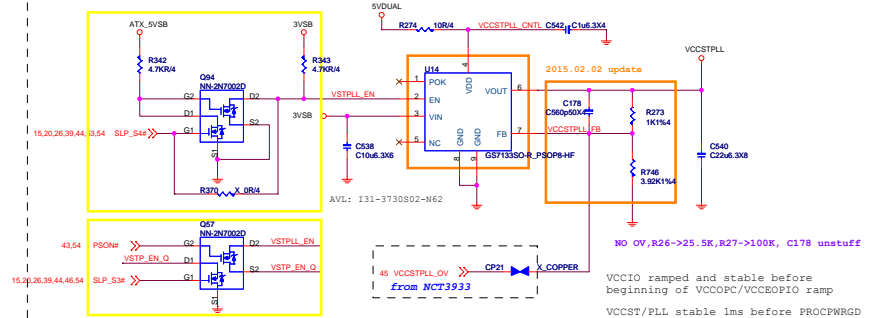


VCCSTPLL

1.0V; 250mA

For Cost down VCCST4VCCPLL merge

for Gaming3/5, Classic, ECO and H110

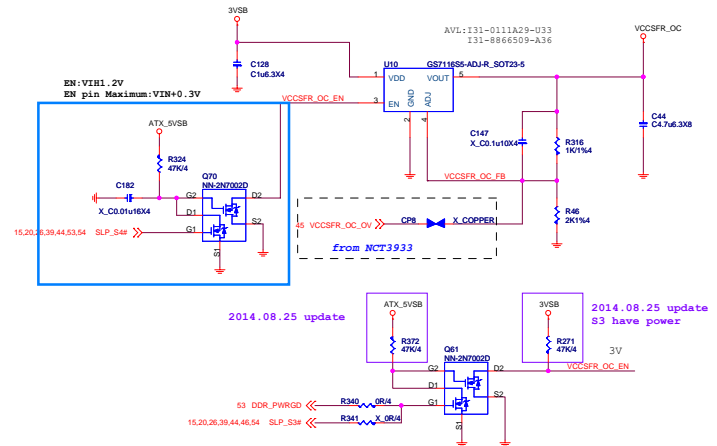


To solve CPU hotplug and lake current

VCCPLL_OC

1.2V; 110mA

2014.08.21 update



PCB

P/N: PD0-0798420-G37
PD0-0798420-E48

CPU Socket

CPU_H1
CPU
CPU_H1

Battery

BAT1_X1
BAT-BCR2032P-RH

Audio Small Cover

COVER1
Audio
Cover
E21-7978010-RH

LAN Cover

COVER2
Audio
Cover
E21-7978010-RH

USB3.1 Label

USB31_LA1
Label
LA1 LABEL

Gaming Network Manager

NET_LA1
Label
[297-Gaming]
Y02-MU00170-CFO

for GAMING Pro sku+Krait sku

SSE

SSE_LA1
Label
[297-Gaming]
Y02-MA00101-SSE

SBC Label

SBC_LA1
Label
[297-Gaming]
X_SBC LABEL

HDMI Label

HDMI_LA1
Label
HDMI LABEL

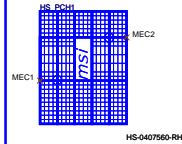
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AML_LA1
Label
BIOS_LABEL
BIOS_LABEL

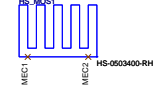
Marketing Label

Z170_LA2
Label
[297-Gaming]
MKT-LABEL
Z170_LA1
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MKT-LABEL
Z170_LA3
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[297-Gaming]
MKT-LABEL

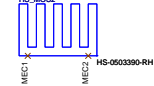
PCH Heatsink



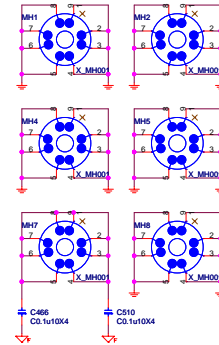
MOS1 Heatsink



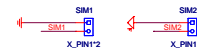
MOS2 Heatsink



Mounting Holes



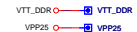
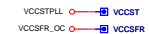
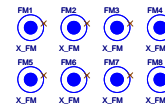
Simulation



Test point



Optical Fiducial Marks-120




MICRO-STAR INT'L CO.,LTD

MS-7A11

Site	Document Description	Rev
Custom	Manual parts	1.0
Date: Friday, September 25, 2015	16:58:00	67 of 68





MICRO-STAR INT'L CO.,LTD		
MS-7A11		
Site	Document Description	Rev
Custom	XDP&EMI CAP	1.0
Date: Friday, September 25, 2015		Sheet 68 of 68